Two Stage OP Amp Design

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1. INTRODUCTION

This project presents the design and layout of a two-stage operational amplifier (op amp) with a buffer stage that meets the given specifications. Op amps are commonly used in the electronic industry for their versatility [1]. They can offer high gain, high input impedance and low output impedance [2]. There can be many factors to consider in op amp design and it can be complicated for certain applications. Layout is especially an important stage in the design and can present its own unique challenges.

2. CIRCUIT DIAGRAM AND OPERATION

2.1 Circuit diagram

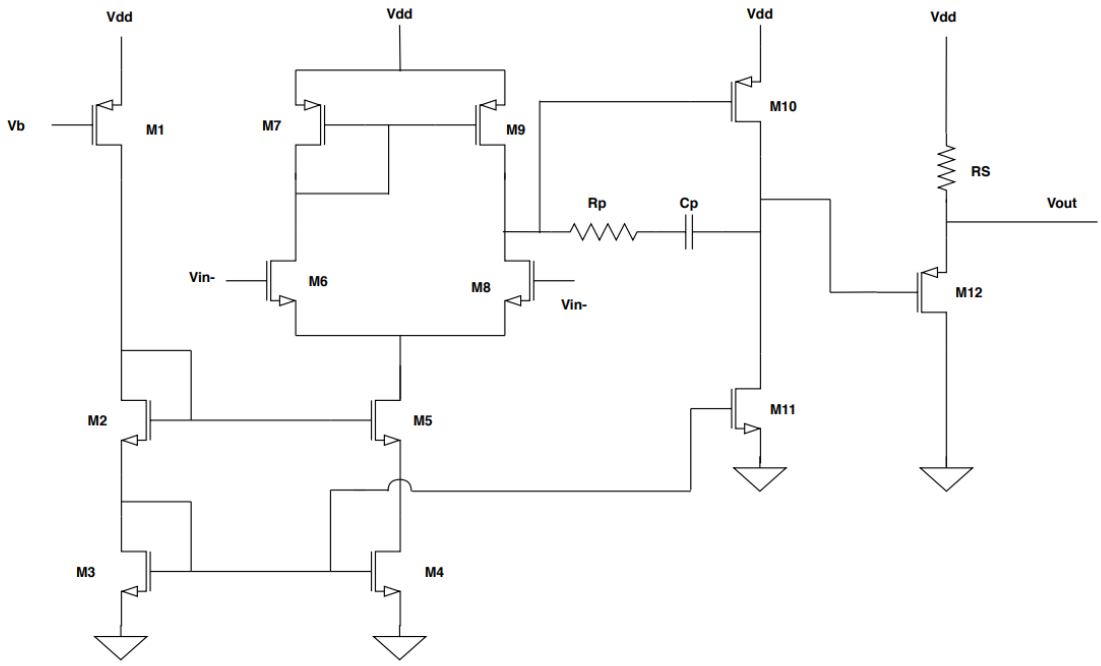

Figure 1: Circuit diagram of op amp

Table 1: Op amp component parameters

Component	Size (WxL in um)	Component	Value
M1	30, .6	M9	60,.6
M2	10,.6	M10	120,.6
M3	10,.6	M11	30,.6
M4	30,.6	M12	135,.6
M5	30,.6	Rp	4.1k ohms
M6	10,.6	Cp	1.8p
M7	60,.6	Rs	499 ohms
M8	10,.6		

Table 2: Op amp DC bias values

Bias voltage	Value	Bias voltage	Value
Vdd	1.8V	Vb	1.25V
Vin- (dc portion)	1.5V	Vin+ (dc portion)	1.5V

2.2 Circuit operation

The op amp in figure 1 is composed of 4 key components. The first stage is a single ended differential amplifier composed of M6, M7, M8, and M9. The purpose of this stage is to provide the majority of the overall amplification for the differential signal while also significantly attenuating the common mode signal. The current mirror load was chosen as it allows the differential amplifier to output a single ended signal while maintaining a high gain.

The differential amplifier stage outputs into a common source amplifier composed of M11, acting as a current source, and M10 acting as an amplifier. This stage provides the remaining amplification while allowing for a wide output swing.

The output stage located on the far right is a common drain amplifier and consists of M12 acting as an amplifier with a resistor load. The purpose of this stage is to serve as a buffer, lowering the output impedance and increasing the drivability while providing unity gain.

M1 M2 M3 M4 and M5 serve as a biasing stage and form a current mirror where the current in M5 and M4 is approximately three times the current on the left, M2 M3, side. Rp and Cp are needed as part of miller compensation, these components determine the pole locations in the frequency response [3].

2.3 Bias Points

The DC operating points of each transistor are given in table 3. To ensure linearity, each transistor operates in the saturation region.

Table 3: DC operating parameters

Component	Id (uA)	Vds (V)	Power (uW)
M1	21.1	-.558	11.8
M2	21.1	.691	14.6
M3	21.1	.55	11.6
M4	62.1	.545	33.8
M5	62.1	.191	11.9
M6	31.08	.534	16.6
M7	31.08	-.529	16.4
M8	31.08	.534	16.6
M9	31.08	-.529	16.4
M10	-64.2	-.899	57.7
M11	64.2	.9	57.8
M12	-420	1.59	667.8

3. LAYOUT

3.1 Layout

The complete layout of the entire op amp has an area of 24960 um^2 and is shown in figure 2. The layout consists of three major blocks. The first block is the current mirror consisting of M1, M2, M3, M4 and M5. This block is shown in figure 3 and has an area of 1386 um^2. The next block is the differential amplifier consisting of M6, M7, M8, and M9. This block is shown in figure 4 and has an overall area of 1027 um^2. The miller compensation circuit consisting of Cp and Rp is also shown in figure 4. Due to the large capacitance of Cp, two capacitors in parallel, both with a width and length of 30um, are used to achieve the necessary capacitance value. The final block is shown in figure 5 and consists of M10 and M11 which make up the common source amplifier in addition to M12 and Rs which make up the common drain amplifier. The total area for this block is 3841 um^2.

During the layout process, special care was taken to make the differential amplifier as symmetric as possible to maximize CMRR. The lengths of the interconnects were kept to a minimum to reduce parasitics and long interconnections had relatively large widths to reduce their resistance. Furthermore, the layering of different metals was generally avoided to reduce parasitic capacitances.

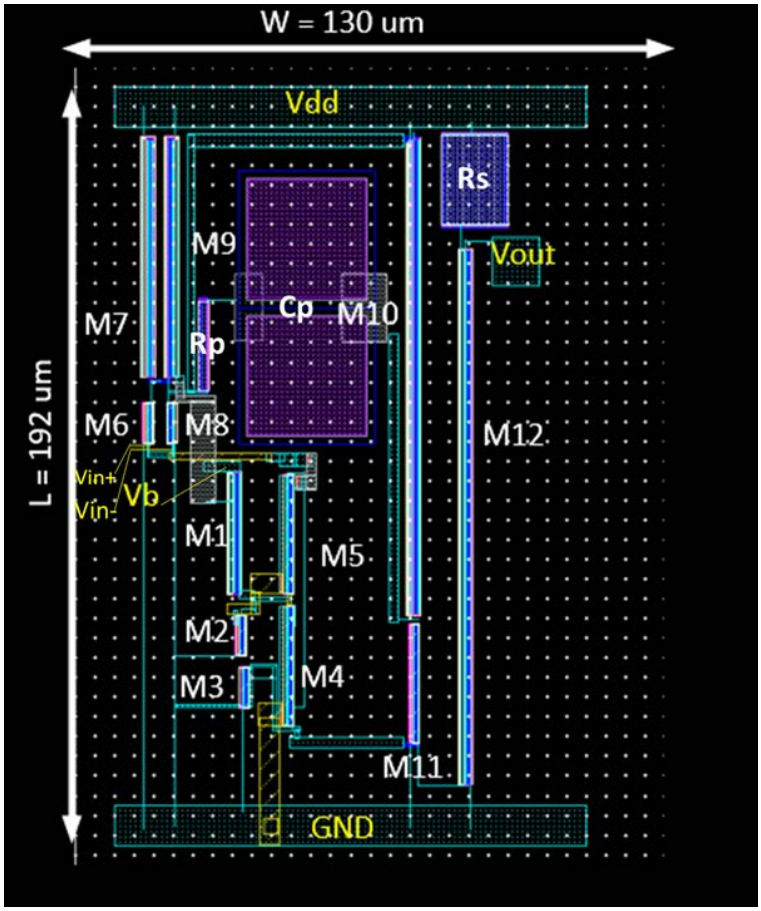

Figure 2: Layout of op amp

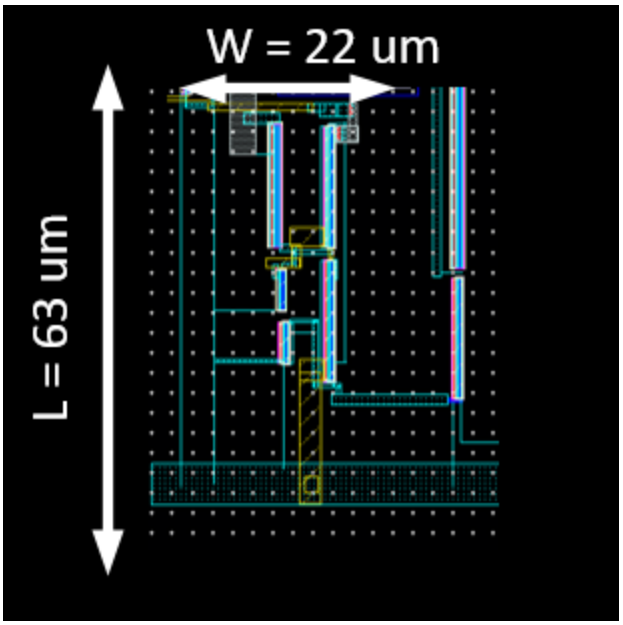

Figure 3: Layout of current mirror

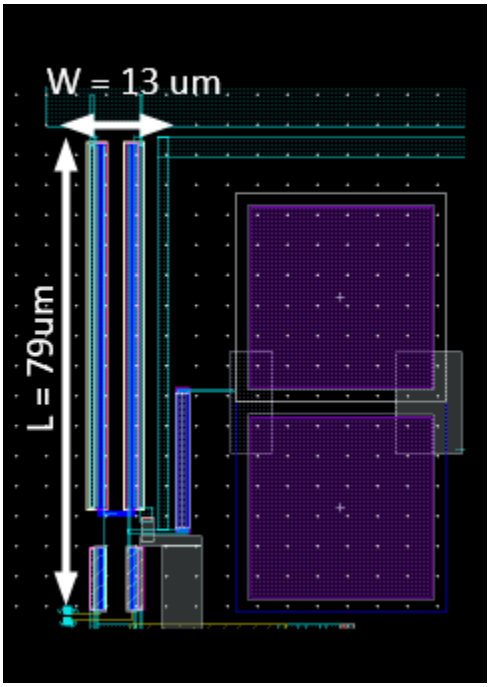

Figure 4: Layout of differential amplifier stage

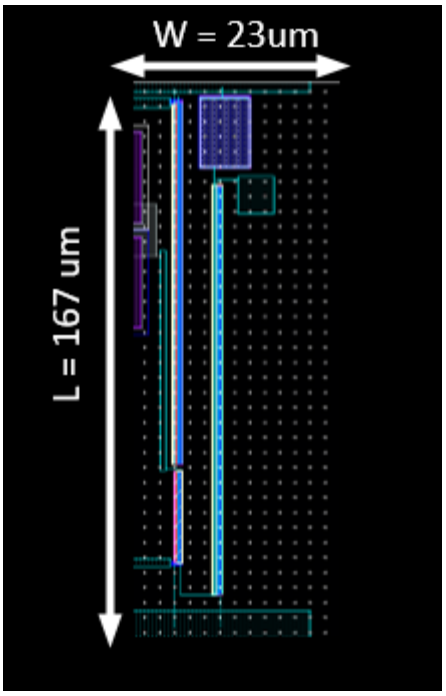

Figure 5: Layout of common source and common drain stage

3.2 Layout Issues

The layout was sufficient in that all project specifications were met. However, the layout is still not optimal. It could be much more compact, and this will likely minimize parasitics and lower the cost of the circuit if it were to be manufactured. Transistor fingers could have also been used to lower parasitic effects.

4. POST LAYOUT SIMULATIONS

4.1 Post-layout simulation results

The plots for each specification are shown in figures 6 and 7. Figure 6 shows the DC gain, unity gain bandwidth, phase margin, CMRR, PSRR, input impedance, and output impedance of the circuit. Meanwhile the swing can be calculated to be .837 V and the phase margin can be calculated to be 20.1V/us from figure 7 and the below equation. Lasty, the DC analysis of the circuit showed that its power supply had a current output of 468.6uA.

$$SR = \frac{.9V_{DD} - 1.1V_{out,min}}{\Delta t}$$

Due to the special considerations made during layout, the post-layout simulations met the requirements and no modifications to the circuit or layout were needed.

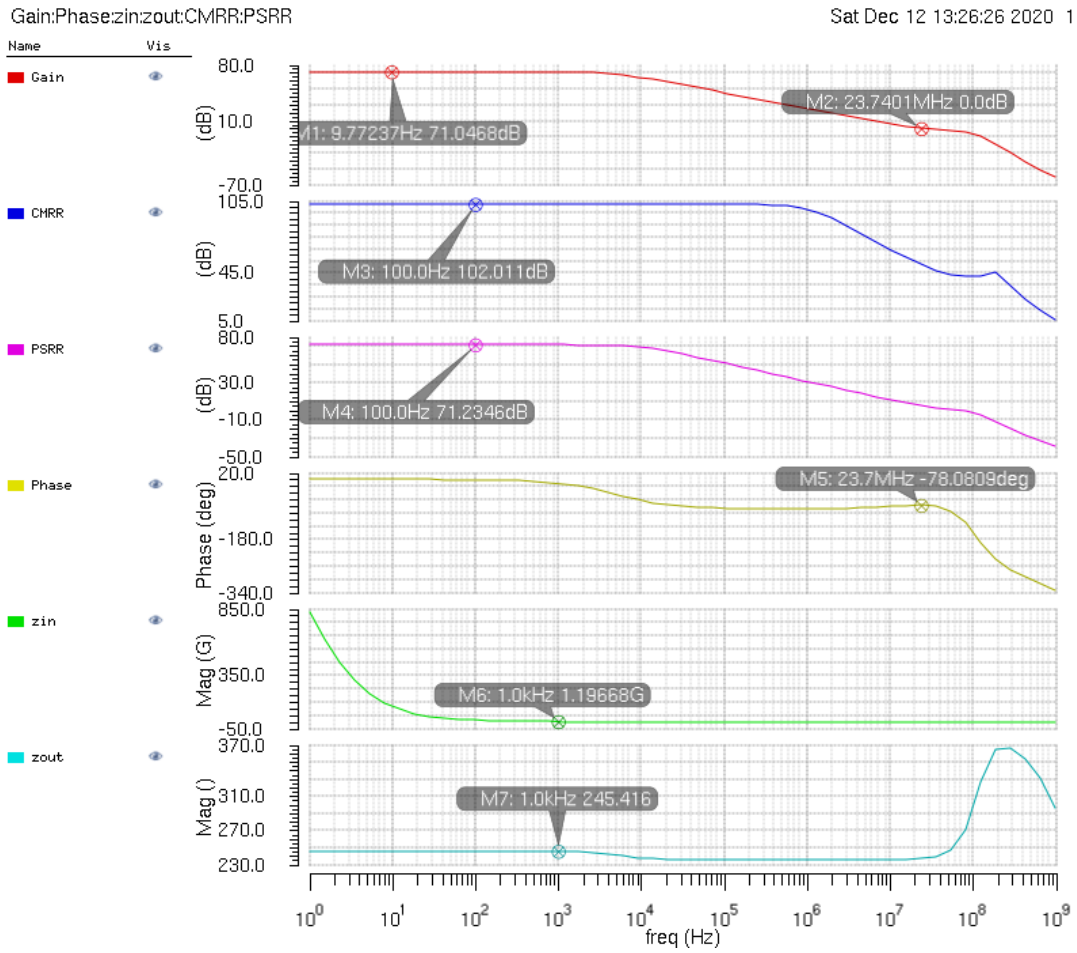

Figure 6: Post layout gain, CMRR, PSRR, phase, input impedance, and output impedance plots

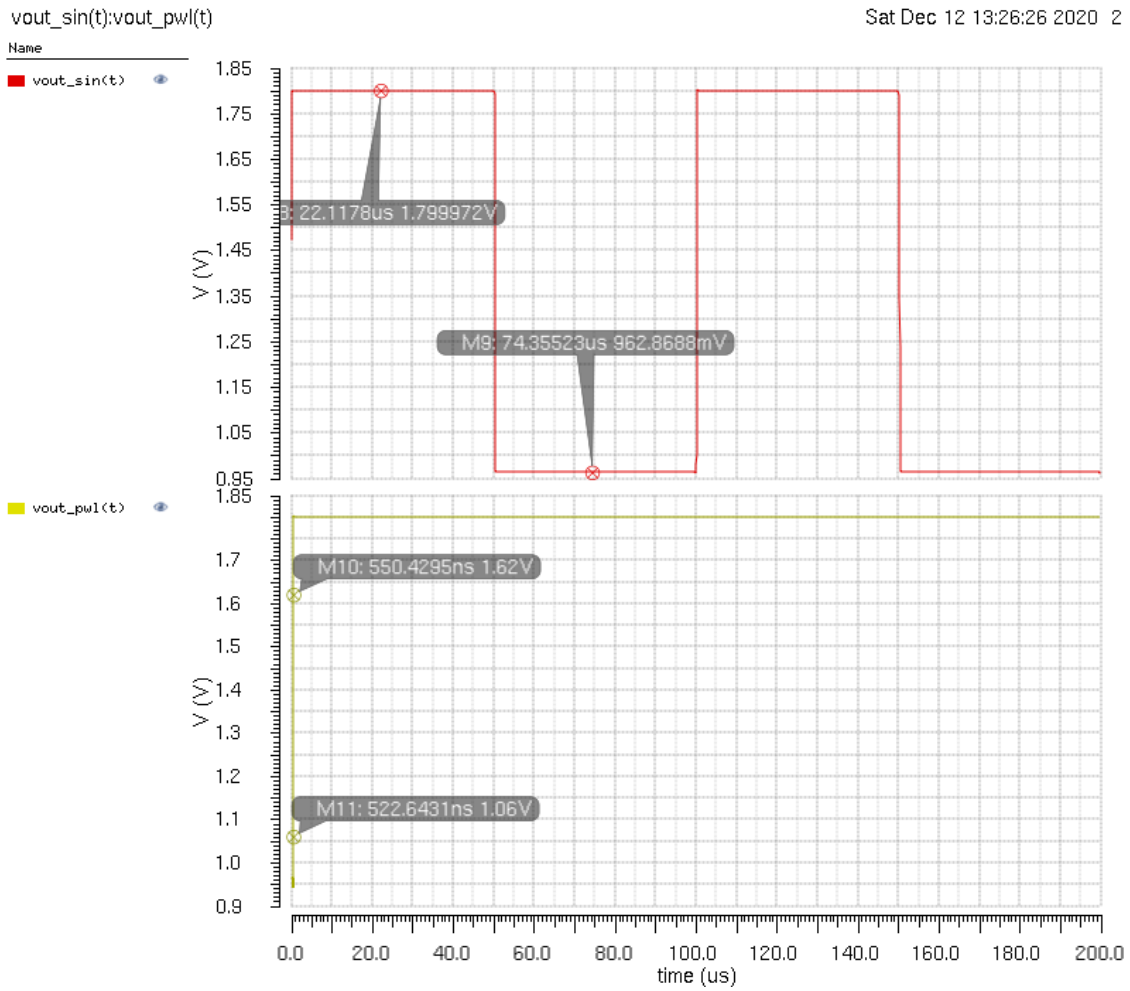

Figure 7: Post layout swing and slew rate plots

4.2 Post-layout simulation issues

Fortunately, no design adjustments or technical issues were faced generating the post layout results. Performing LVS resulted in a warning about ambiguity points related to the capacitors but on further inspection, they had been resolved correctly.

5. PERFORMANCE

5.1 Performance summary

Table 4 summarizes the pre-layout and post-layout simulation results.

Table 4: Pre and post layout performance summary

Item	Specification	Circuit level simulation	Post layout simulation	Post layout simu. meets specification (Yes or No)
DC gain V_{out}/V_{in}	> 50 dB or 316 (must meet.)	70.8dB	71.0dB	Yes
Unity-gain bandwidth:	> 20 MHz (must meet)	30.5 MHz	23.7MHz	Yes
Power dissipation:	< 2 mW (must meet.)	1.02mW (568uA,1.8V)	.843mW (468.6uA at 1.8V)	Yes
Phase margin:	> 90^o at the unity-gain frequency	108.2 degrees (-71.8+180)	101.9 degrees (-78.1 +180)	Yes
Slew rate*:	> 20 V/µsec for low-to-high change	22.5V/us	20.1V/us	Yes
CMRR:	> 90 dB at 100 Hz	115.0dB	102.0dB	Yes
PSRR:	> 60 dB at 100 Hz	74.7dB	71.2dB	Yes
Input impedance Z_{in} :	> 50 MΩ at 1 kHz	614.1Mohms at 1KHz	1.2 Gohms	Yes
Output impedance Z_{out}:	< 500 Ω at 1 kHz	189.9 ohms	245.4 ohms	Yes
Output swing voltage:	> 400 mV peak-to-peak	.846 V peak to peak	.837 V peak to peak	Yes

5.2 Possible improvements

All the specifications were met however the layout could be redone to achieve a closer phase margin to the schematic results. Since all of the performance requirements were met, the design could have been improved through a smaller layout area. This could have been achieved through better placements of the circuit components as well modifications to the components parameters. Namely the size of Cp, M12, and M10 could have been reduced to reduce the overall area of the layout while sacrificing some of the performance of the op amp.

6. SUMMARY

In summary, the op amp layout and schematic made all the specified criteria. This project allowed us to gain a better understanding of the tradeoffs and important factors in analog

design as well as practice using the Cadence design environment. A possible future recommendation would be to give students a choice in the project topic. They could design an op amp, or a different type of circuit such as an analog multiplier, oscillator, or OTA. This would give students the opportunity to learn about other types of circuits that we didn't get a chance to deeply study.

7. References

[1] D. Neamen, *Microelectronics Circuit Analysis and Design*, 3rd ed.
[2] B. Razavi, *Design of Analog CMOS Integrated Circuits*
[3] Iowa State University, *Design of two stage op amp with miller compensation*

8. Appendix

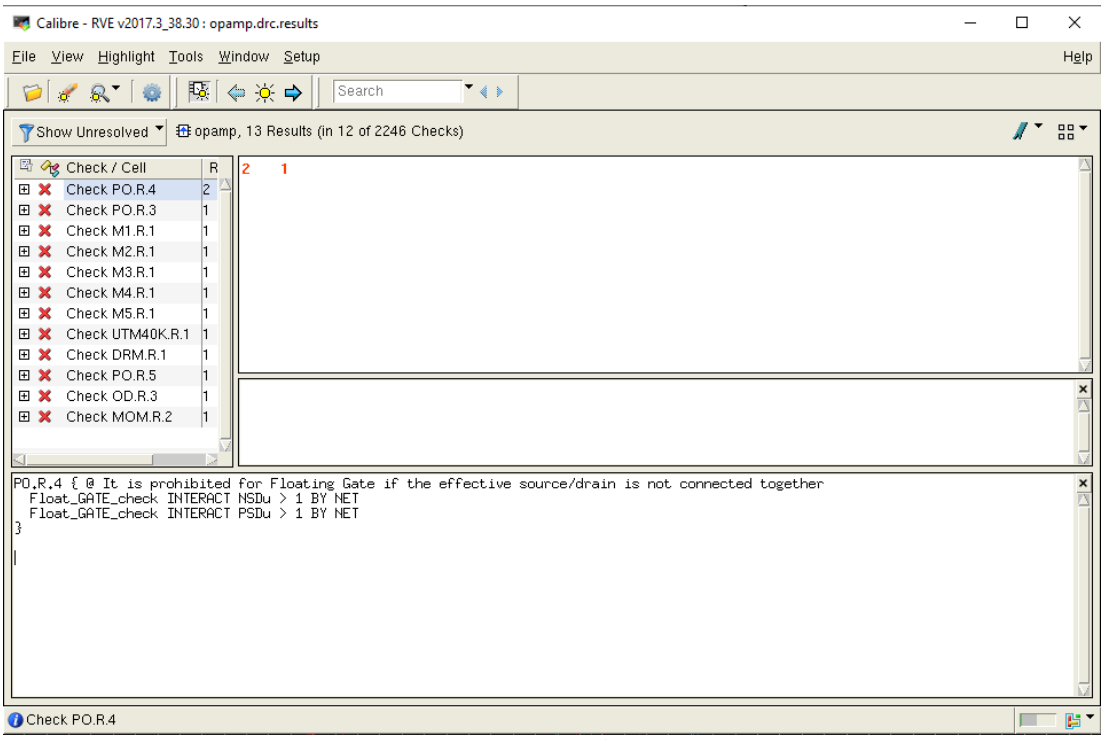

Figure A: Screenshot of DRC results

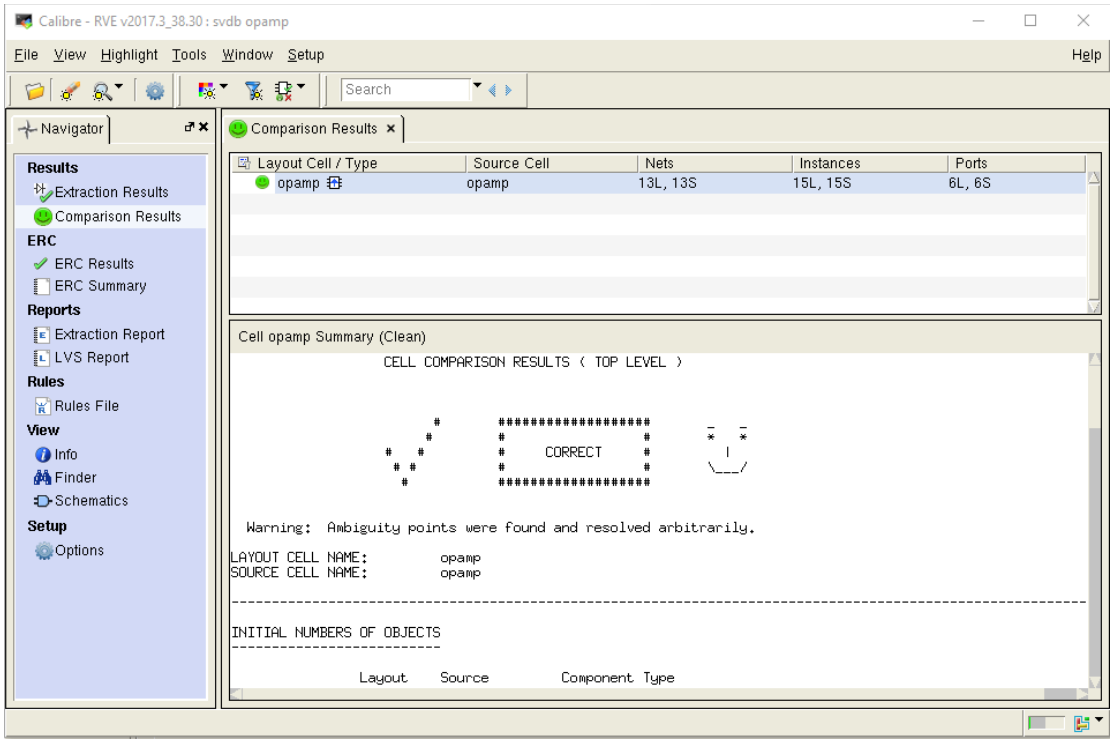

Figure B: Screenshot of LVS results

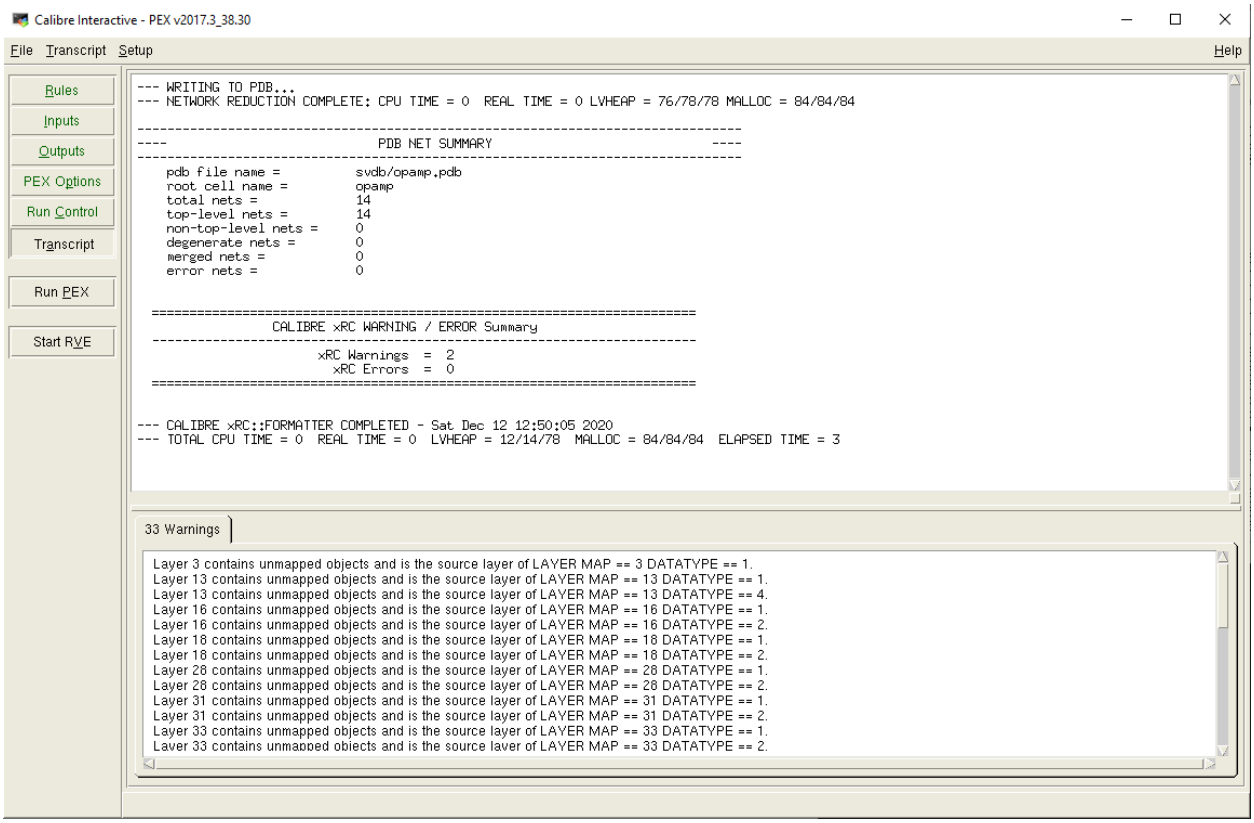

Figure C: Screenshot of PEX results

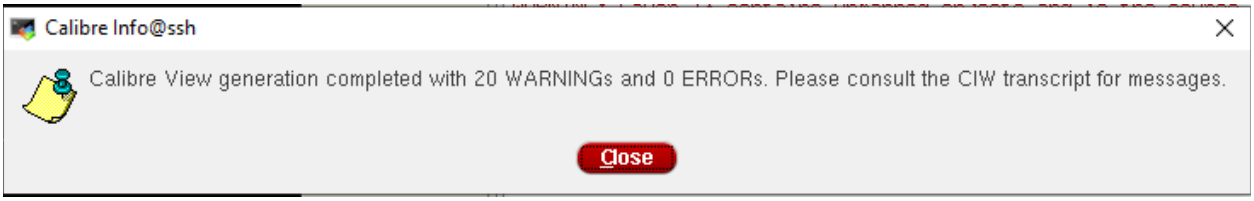

Figure D: Screenshot of Calibre view generation